**Microprocessor and Interfacing (ICE-3101)**

* **Chapter Zero (Computer number system,codes and Digital Devices)**
* Hexadecimal conversion
* BCD
* Table (ASCII Code)
* **Silde-1(History of Microprocessor)**
* Von Neumann Architecture (self study)
* Harvard Architecture(self study)
* Risc and cisc(difference)
* Defination and theory (year wise)
* **Slide-2(8086 Internal Architecture)**
* **Silde-3 (Pin diagram of 8086)**
* Memory Banking
* **Chapter-8(Semiconductor and interfacing)**
* Types of memory
* Types of ROM and its characteristics
* Types of RAM and its characteristics
* Error detection and correction(Hamming code)
* **Chapter-9(I/O Modes and Interfacing)**
* I/O device
* Peripheral device
* Controllers
* Device
* I/O modes
* I/O mapped
* Memory mapped
* Programmable I/O modes,advantages,disadvantages
* Interrupt mode,advantages,disadvantages
* 8086 interrupts and interrupt responses
* 8086 interrupt types(0-5)
* Priority of 8086 interrupt
* Basic 8253 and 8254 operation
* Initialization of an 8254 programmable peripheral device
* 8259A overview and system connection
* Initialization of an 8259A
* 8254 counter mode and application
* Difference between 8254 and 8253
* **Chapter-1 (marut)**
* Adv of high level language
* Adv of assembly language
* **Chapter 3 – (Marut)**
* Organization of pc (3.3)
* The opertating system(3.3.1)
* Start up operation(3.3.4)
* **Chapter 4 – (Marut)**
* Assembly Language Syntax ( 4.1,,,,4.1.1 to 4.1.4)
* Program Data (4.2 )
* Variables (4.3,,,4.3.1,4.3.2,4.3.3(character strings))
* Named Constants (EQU)(4.4 )
* A Few Basic Instructions (4.5)
* MOV(4.5.1)
* ADD, SUB, INC, and DEC(4.5.2)
* Translation High-Level Language to Assembly Language(4.6)
* Memory Models(4.7.1)
* Data Segment(4.7.2 )
* Stack Segment(4.7.3)
* Code Segment(4.7.4 )
* Input and Output Instructions (4.8)
* INT 21h(4.8.1)
* A First Program (1.9 )
* FIG-4.8
* Displaying a String(4.11 )
* A Case Conversion
* Program(4.12 )
* Exercises(LAB)
* **Chapter 6 – (Marut)**
* An Example of Jump(6.1)
* Conditional Jumps (6.2)
* The JMP Instruction (6.3)
* Branching Structure-s(6.4.1 )
* Looping Structure(6.4.2)[ FOR LOOP, WHILE LOOP]
* Exercises(LAB)
* **Chapter 7 – (Marut)**
* Logic Instructions (7.1)
* AND, OR, and XOR Instructions (7.1.1)
* NOT Instruction(7.1.2 )
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* Shift Instructions(7.2)
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* **Chapter 10 - Marut**
* Addressing modes(10.2)
* Register indirect mode(10.2.1)
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**DMA(Direct Memory Accesss) (Both MP and interfacing and embedded)**

* **Chapter-9[Hall Book]**
* DMA definition
* DMA operation
* Block diagram of DMA controllers
* DMA transfer
* Non burst mode
* Burst mode
* Adv. And disadv.
* Case study of 8237 dma controllers
* Independent auto initialization of all channels
* Working of dma controller
* Interfacing a floppy disk to 8086 through 8237 dma controller
* i/o channels
* dma vs i/o channel
* limitation
* i/o processor

**Chap-13(dma,dma controlled i/o)(barrey b. brey)**

* Basic dma operation(fig-13.1)
* 8237 dma controller(fig-13.3)
* Disk memory system
* Floppy disk memory(self study)